ADVANCE PROGRAM OVERVIEW (Program details are tentative and may change)

	Please note that the oral presentations	s listed below are provisional and subject to contere	ance registration. Additional oral presentations are	currently withheld due to authors' pending registra	tion or final decisions regarding whether they will b	be presented as oral or poster sessions	
08:00am-08:55am	DVY : Deaster 1 2004 (Faceford Registrian						
Venue			Gand				
09:00am - 09:15am 09:15am - 10:00am			Opening Dr Vic Lin Jing-Cheng,				
10:00am - 10:45am	A EL TRUCE U MARING A PARET. L'IN POUR D'ANTRA DE L'ANTRA DE L'ANT						
10.45am - 11.00am 11:00am - 12:30pm			Cottee/ Panel Session: Asia's Role in the Global Semic Decisity Andrew Cote 5 on Ferenative Cone Sec.	Tea Break Orductor Industry (Moderator: Keat Yap, Kearney) Orductor Industry (Moderator: Keat Yap, Kearney) Orductor Industry (Moderator: Keat Yap, Kearney)			
12:30pm - 1:30pm Venue		Lands Const Database Const Database D 19-94 Wing, VT, Siconsam Resister Mathieut Co., LM					
1:30pm - 2:15pm 2:15pm - 3:00pm		The Decision of the Content of the C					
3:00pm - 3:45pm	ATTENDE AND						
3:45pm - 4:00pm 4:00pm - 5:30pm			Cofee/Tes Break (Panel Session: The Role of Co-Packaged Optics in Advancing Al				
6:00pm - 8:00pm							
Venue	Veranda I	Veranda II	DAY 2: December - Versinda II	4, 2024 (Wechenday) Rhearfront I	Riverfront II	Riverfront E	
08:30am - 10:15am	PDC1: Failure Analysis of Advanced Packages: Fundamental, Skills, Philosophy & Case Studies	PDC2: Photonic Technologies for Communication, Sensing and Displays	PDC3: Water Bonding for Advanced Packaging Applications	PDC4: Current and Future Challenges and Solutions in Al & HPC	PDC5: Mechanics and Reliability of Lead-Free Solders Joints	PDCE: Chiplet, Heterogeneous Integration and Co-Packaged Optics	
10:15am - 10:30am	Dr Yong-Fen Haieh, MA-Tek	Dr Torseten Wpiejewski, Husevel	Dr Viorel Dragoi, EV Group Coffee/T	Dr Retsi-Ahmed Garral, AMD	Professor Jeff Subling, Aubum University	Dr John H. Lau, Unimicron Technology Corporation	
10:30am - 12:00pm Venue	PDC1 (contid)	PDC2 (contid)	PDC3 (contid) WaterFrom	PDC4 (contid) 4 Bail Room	PDCS (conifd)	PDC6 (confid)	
12:00pm - 1:30pm			EEE EP	Luncheon			
1:30pm - 2:15pm	Putars Starting Lync, Borgodiar Nunan, OlfA Starting Distances Backward, Backward Backward, Backw						
2:15pm-2:45pm 2:45pm-4:15pm	R to Caper Caure Medrag (Avends) Edubtors Preventions @ Revetors in and in a constraint of a						
4:15pm - 5:15pm Venue	Veranda I	Veranda B	Interactive Poster Presentation 1 / Exhi Veranda II	blion / Coffee Break @ Waterhort foyer Riverfront I	Riverfront II	Riverfront B	
5:15pm - 6:15pm	TBC	TBC	TBC	TBC	TBC	TBC	
6:30pm - 8:00pm				quet Dinner 5, 2024 (Thumday)			
Versae	Veranda I Invited Talk 1: Jamos Papanu, TEL	Veranda II Invited Talk 2: Tan Yik-Yee, Yole Group	Veranda II Invited Talk 3: Sidina Ware, eV-Technologies	Riverfront I Invited Talk 4: Chan Pin Chong, Kulicke & Sotta	Riverbont II	Riverfront II	
09:00am-09:30am	Invited Talk 1: James Papanu, TEL D2W Hybrid & Fusion Bonding to Enable Adv Packaging (1313)	Glass Core Substrate Market and Opportunity	Invited Talk 3: Sidina Wane, eV-Technologies Smart Integrated Electromagnetic Skina	Invited Talk 4: Chan Pin Chong, Kulicke & Sotta Fludess TCB for Chiplet Integration	Invited Talk 5:	Invited Talk 5:	
	Hybrid and Fusion Bonding 1 1187. Improved Edge Datedion Algorithm for Blumed Algorithm Marks in Hybrid Bonding	Wafer Processing and Characterization 1 1412. Comprehensive Die Direngfes Comparisons for Glass using Different	Emerging Technologies	Advanced Packaging 1 1255. Defluxing in Advanced Packaging: Critical Process Considerations	TSV and Wafer Level Packaging 1 1191. Optimizing fabrication processes to improve resistance in Via-Last	Thermal Management and Characterization 1 1103 Power Management IC device efficiency & thermal study	
	Hybrid Bonding Samaung Japan Corporation	1412. Comprehensive Die Strengths Comparisons for Glass using Different Singulation Methods DISCO Corporation, USA	1128. Generation of Beam Profiles from Chip-to-Pree-Space Coupling using Deep Neural Network Nanyang Technological University, Singapore	ZESTRON ATERCES	1191. Optimizing tabrication processes to improve resistance in Via-Last TSV for BSI applications Institute of Microelectorrics, Singapore	NXP Semiconductor Company, China	
09:30am -10:30am	1125. Post-CMP Clean Optimization for SICN Hybrid Bonding Applications Institute of Microelectronics. Singapore	1410. Nobium-last Process for Multi-foundry-compatible Water Level Processing of Superconducting Interposers Institute of Microelectronics. Singapore	1253. Feasibility and Performance of Fully Additive Manufactured Light Boltes Friedrich-Alexander Universität Erfansen Nimbero	1342. ECC-based Flux Cleaning Monitoring for Improved Reliability in Advanced Packaging Products TSMC. Taiwan	1227. Utilizing Ensemble Learning on Small Database for Predicting the Reliability Life of Water-Level Packaging National Taino Hua University. Taiwan	1135 Thermal design and analysis of a flip-chip GaN-on-SIC HEMT Institute of Microelectronics. Sincepore	
	1283. FEA of the Effect of Structural Parameters and Maslignment on Bonding Strength in FP Hybrid Bond	1288. 200mm Reconstituted Wafer for Fan-out of Microfiuldics and CMOS Electronics	1377. Innovations and Challenges in Laser Direct Structured Mechatronic Integrated Devices for Aviation	1262. Dual Damascene process for 500m RDL using High Resolution Photosensitive Polymer	1344. Accelerating Overlay Error Optimization in Fine-Pitch Water-to-Water Hybrid Bonding through ML	1163 Silicon-Based Micro-Fluid Cooler Package Integration for High Performance Computing	
10:30am - 10:45am	Tainghua University, China	IMEC, Belgium	Lehrshuhl für Fertigungsautomatisierung und Produktionssystematik Cotise/T	MEC, Belgium	Institute for Infocores Research, Singapore	Institute of Microelectronics, Singapore	
Venue	Veranda I Hybrid and Fusion Bonding 2	Veranda II Water Processing and Characterization 2	Veranda II Thermal Interface Materials	Riverfront I Advanced Packaging 2	Revenant II TSV and Water Lavel Packaging 2	Riverfront II Thermal Management and Characterization 2	
	1336. Process Development of Chip to Wafer Hybrid Bonding with Polymer Passivation	1352.CMOS compatible 2D material integration for Sensor Applications on 200mm waters	1113. Evaluation of TIM Cross-Sectioning Methods on Lidded High- Performance Microprocessors	1357. Investigation of UBMRDL Contact Resistance Based on ICP Sputter Etch Conditions and Ortical Design Dimensions	1360. Investigation of Parasitic Surface Conduction Effect on Interposers for 2.5D/3D Heterogeneous Integration	1171. Effect of Contact Characteristics on Thermal Contact Resistance of Grease-Jess Uniform Contact Surfaces	
10:45am -11:45pm	Institute of Microelectronics, Singapore 1368. Process flow and requirements for fusion bonding of photonic interposers with ultra-thin dielectric layers	INEC, Belgium 1384. Hyperspectral Component Fabrication on 200mm CMOS Image Sensor Water	AND, Singspore 1225, Selection of Non-clean Flux for Metal TM	Evatec AG, Switchasland 1348. Packaging technology for Sub-tenshertz antenna in module	Institute of Microelectronics, Singapore 1370. Embedded defect depth estimation using NIR Model-less TSOM	KOA Corporation, Japan 1274. Real-time Evaluation of Effective Thermal Conductivity Profile for the Redistribution Layer (RDL)	
	Institute of Microelectronics, Singapore	MEC, Belgium	Siliconware Precision Industries Co., Ltd., Talean	Shinko Electric Industries Co.,Ltd, Japan	Kongju National University, South Konaa	HPC, A'STAR, Singapon	
	1316. Parylene as an adheaive for water and chip bonding as well as for applications in water level packaging Fraunhofer Institute for Electronic Nano Systems	1390. Characterization of Carbon Contained Films at Bonding Interface for the Application of Backside Power Delivery Networks Yokohema National University, Japan	1125. Analysis of Indium-Silver Aloy Thermal Interface Material Reliability and Coverage Degradation Mechaniams Arrivor, Yones	3509. Precise Wavelength Control in Fabry-Perot Filters using Thin Elch Stop Layers MEC, Belgium	1373. Study of Direct Copper Electroplating on Ruthenium Seed Layer for TSV Processes at 300mm Wafer Level Institute of Microelectronics, Singapore	1282. POD-ANN Thermal Modelling Framework for Rapid Thermal Analysis of 2:5D Chiplet Designs HPC, A*STAR, Singapore	
Venue 11:45pm -1:00pm			WaterFro	nt Baliroom			
Venue	Veranda 1	Veranda II	Versinda II	Riverfront I	Riverfront II	Riverhont II	
1:00pm - 2:00pm	Electrical Simulations & Characterization 1	Wireless and Antenna Package Designs	Sponsora' Presentatio Materials and Processing 1	na @ Riverfront II and III Mechanical Simulation & Characterization 1	TSV and Wafer Level Packaging 3	Thermal Management and Characterization 3	
	1108. Signal integrity analysis of darse wire channels on 2.5D substrate technologies for UCIe and BOW applications	1139. Development of 2.4GHz band L-shaped Circular Polarized slot antenna	1118. New DA Adhesive Meets Challenging Performance, Reliability and Cost Objectives of Automotive MCU Packaging	1147. Advanced Prediction Model for SACQ Solder Reliability Assessment for Automotive Memory Applications	1396. Digital Lithography in Patterning of UHD FoWLP Utilizing Novel PI Dielectrics	1343. Optimizing Chiplet Placement in Thermally Aware Heterogeneous 2.5D Systems Using Reinforcement Learning	
2:00pm - 3:00pm	Institute of Microelectronics, Singapore 1167: Equivalent Electromagnetic Radiation Model of Chip Based on Near- Field Scanning for EM Analysis in Ceramic SiP	Kyushu University, Japan 1203. Development of Long-Range Weeksa Energy Harvesting Circuit by Melinitare ContemplaWeiten Contempl	Henkel, USA 1159. Photosensitive aquecus alkaline developable magnetic material for inductor and balun transformers in 3D WLP	Micron Semiconductor Asia Operations 1324. Copper balance and water level warpage control and effect of package atreas and board-level TC acidar joint reliability	EV Group, Austria 1374. Panel Level Fine Patiening RDL Interposer Package	Institute for Infocomm Research, Singapore 1354. Efficient Thermal-Aware Floor-planning with Bayesian Optimization: A Simulation, Winter Assessed	
	UESTC, China	Kyushu University, Japan 1307: A Connect fud Antenna Array with Resemble Reservice NG milimates	FUJFILM Corporation, Japan	Institute of Microelectronics, Singapore	Samung Bectronics, South Korea 1953, Chin In Water and Water In Water Dennity antimation and Design	Institute for Infocomm Research, Singapore 1111. Charities the Next 5, 10 & 20	
	1161. Design of underground structure cover with self-complementary sits for wireless telecommunication application Kyusu University, Japan	1307. A Compact to4 Antenna Ansy with Steenable Beam for 5G millimeter- Wave Smatphone Applications ASE Group, Taiven	1173. Enhancing Device Performance through Non-Pressure Sintering on Copper Lead frames Henseus Materials Singapore	1340. Material sensitivity of a fan-out package waspage – simulations and experimental validation Institute of Microelectronics, Singapore	1193. Ohip to Waler and Waler to Waler Density estimation and Design rules physical verification. Institute of Microelectronics, Singapore	1111. Charling the Semiconductor Industry's Path Over the Next 5, 10 & 20 Years AND, USA	
3:00pm - 4:00pm	Electrical Simulation & Gauscientization 2 Maintain and Processing 2						
	1223. Effect of Meah Ground Plane on Impedance Control and Crosstalk of Organic Interposers Targeted for Chiplet Applications					Embedded and Fan-Out Packaging	
		1126. Investigation of the Electromigration Behaviour of Solder Bump under Different Conditions	1176. Analysis of Basic Properties and Bonding Properties of Various Melting Temperature Solders	1181. Evaluation of Thermo-mechanical Fatigue life of Microvias under PCB Substrate's influence during Reflow Process	1405. Splitting Process Integration for 2.5D/3D Packaging	Embedded and Fan-Out Packaging 1131. The FOShipili technique - a low cost solution for the ship level ten- out on substrate package	
4:00pm - 5:20pm	AST, Japan 1355. Signal Integrity Simulation and Analysis for 2.5D Advanced Package Intercorrect Based on UCIa	1126. Investigation of the Electronignation Behaviour of Solder Bump under Different Conditions Nexperis, Hong Xong 1146. Assembly of Multi-Device Power Package with Clips as Interconnects	MKE, South Konea	Yokohama National University, Japan	1405. Splitting Process Integration for 2.5D/DD Packaging Institute of Microelectronics, Singapore	1131. The #OStript/technique - a low-cost solution for the ship level ten- out on substrate package Kore Semiconductor Co., Ltd., Talwan	
	AST, Japan 1355. Signal Integrity Simulation and Analysis for 2.5D Advanced Package Intercorrect Based on UCle MECAS, Corea 1109. Electrical Characterization and Relability Studies of TSI with S-layer	Nesperis, Hong Kong 1146: Assembly of Multi-Device Power Package with Clips as Interconnects Institute of Microelectronics, Singapore	1862, South Korea 1220. Low Flux Residue No Client Soldse Plate for System-in-Package (SP) Appleation Indust. Chres	Yokohama National University, Japan 1205, Impact of Structurel Parameters on the Warpage of IoSGA Packages with Indeem Hermal National Meterial Champite ArtMACuan Intelligent Technology, China	1405. Spilling Process Integration for 2.5000 Packaging Institute of Microsluctureica, Singapore 1303 Maintaing Producting House Boding Generates Optimization in the Chip on Water Process	1131. The FOGspill technique - a fore-cost adultion for the sitip level fae- out on adultative publication of the state of the site of the state of	
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